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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re patent application of:

Steven H. Voldman

Group Art Unit: 2816

Serial No.: 10/631,098

Examiner: Long T. Nguyen

Filed: July 31, 2003

Atty. Docket No.: BUR919990193US2

For: SOI VOLTAGE-TOLERANT BODY-COUPLED PASS TRANSISTOR

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Frederick W. Gibb, III

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANT'S APPEAL BRIEF

Sirs:

Appellant respectfully appeals the final rejection of claims 14, 17, 18, and 24-36, in the Office Action dated November 16, 2005. A Notice of Appeal was timely filed on February 16, 2006.

I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines Corp., Armonk, New York, assignee of 100% interest of the above-referenced patent application.

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II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellant's legal representative or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 14, 15, 17-20, 22, and 24-36 are all the claims pending in the application. Claims 14, 17, 18 and 24-36 stand rejected on prior art grounds. Claims 15, 19, 20 and 22 have been withdrawn from consideration.

Claims 14, 17, 18, and 24-36 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Au et al., hereinafter "Au" (U.S. Patent No. 5,528,188), in view of Brady, et al., hereinafter "Brady" (U.S. Patent No. 5,314,841). Claims 24-30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Ker et al., hereinafter "Ker" (5,631,793) in view of Au in view of Brady. Appellants respectfully traverse these rejections based on the following discussion.

IV. STATUS OF AMENDMENTS

An after-final Response that made no claim amendments was filed on January 12, 2006. An Advisory Action dated January 27, 2006 indicated that, upon filing an appeal, the Response filed on January 12, 2006 did not place the application in condition for allowance, and that the rejections of claims would remain. The Advisory Action also stated for purpose of appeal, the proposed claims filed on January 12, 2006 would be entered. Therefore, the claims shown in the appendix are shown in their amended form as of the January 12, 2006 Amendment.

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V. SUMMARY OF CLAIMED SUBJECT MATER

Independent claims 14 and 31 similarly define a "body that is floating with respect to an underlying substrate " and "gate opposite said body" (item 45 in Figures 5 and 6), "an RC discriminator comprising a resistor and a capacitor" (resistive transistor 42 and capacitor 41 in Figures 5 and 6), and "a circuit control network" (elements 44 and 60 in Figures 5 and 6). Independent claim 24 defines a similar structure, but is more specific to the structure shown in Figure 6 that has the "n-channel SOI MOSFET" and "p-channel SOI MOSFET" (items 43 in Figure 6), the "first" and "second" RC discriminators (items 41 and 42 in Figure 6), as well as the "first" and "second" circuit control networks (items 60 in Figure 6).

Appellant's FIG. 5 illustrates a PFET implementation, which operates as described above except, capacitor 41 and resistive transistor 42 initiate RC coupling of the gate 45. Element 44 acts as a voltage reference which limits the body potential to the reference voltage V_{ref}. In an ESD event, the RC network couples the gate 45 of the pass transistor 43. Similarly, FIG. 6 illustrates a PFET/NFET switch which includes RC networks 41, 42 which operate as described above. In addition, the structure in FIG. 6 includes body limiting devices 60 which limit the body voltage during functional operation. With the claimed invention, as shown in Figures 5 and 6, a pad 40, a capacitor 41, a pass transistor 43, a resistive transistor 42, and element 44, limits the voltage that the floating body can rise to and sets the reference voltage. The floating body 45 of the pass transistor 43 is connected to the input 40 by the RC network (e.g., resistive transistor (e.g., buried resistor) 42 and capacitor 41) such that when a pulsed event occurs (e.g., overvoltage, overcurrent), the voltage of the body 45 rises. This voltage rise of the body element 45 lowers the threshold voltage of the pass transistor 43, which causes the pass transistor 43 to turn on. In this state, the body 45 is dynamically coupled, thereby

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allowing a higher current drive, a lower turn-on voltage and at the same time, less voltage stress.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues presented for review are whether claims 14, 17, 18, and 31-36 are unpatentable under 35 U.S.C. §103(a) over Au et al. (U.S. Patent No. 5,528,188), in view of Brady, et al. (U.S. Patent No. 5,314,841); whether claims 24 -30 are unpatentable under 35 U.S.C. §103(a) over Ker et al., (5,631,793) in view of Au and Brady; and Appellants respectfully traverse these rejections based on the following discussion.

VII. ARGUMENT

A. The Rejection Based on Au and Brady

1. The Position in the Office Action

The Office Action states:

> With respect to claims 14 and 17, Figure 45 of the Au et al. reference discloses a device which includes: a MOSFET transistor (Q1) comprising a gate (gate of Q1), a body (body of Q1); an RC discriminator circuit (32) comprising a resistor (R) and a capacitor (C), and a circuit control network (40) modulating a potential of the body (of M) to provide ESD protection (the circuit of 40 capable of controlling the potential biasing the body of the transistor and therefore it also capable of provide ESD protection) . The Au et al. reference does not disclose that the MOSFET Q1 in Figure 4b is fabricated by using silicon-over-insulator SOI technology However, the Brady et al. reference discloses that silicon-over-insulator (SOI) technology provides advantages over regular silicon

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technology such as increasing the operating speed and reducing the power consumption of the circuitry (Col. 1, lines 12-15). Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify the circuit in Figure 4b of the Au et al. reference by using specific SOI technology to fabricate the MOSFET transistor for the purpose of increasing the operating speed and reducing the power consumption of the circuitry. Thus, this modification meets all the limitation of claims 14 and 17. Note that, in this modification, "the body that is floating with respect to an underlying substrate" on line 3 of claim 14 is met when fabricate the device by using SOI technology (i.e., the body of Q1, Figure 4b in the above modification is floating with respect to an underlying substrate) because the body of an SQl MOSFET is floating with respect to an underlying substrate. Also, note that, the functional limitation in claim 17 is also met as the operation of control network circuitry modulates the potential voltage of the body and limit the body to a reference voltage.

With respect to claims 31 and 32, the modification/combination of Au et al. and Brady et al. as discussed in claim 14 above meets all the limitations of this claim except that the resistor R is a resistive-transistor, However, it is art-recognized that a resistor could be easily implemented in an integrated circuitry by using a transistor that has its gate connected to DC bias so that the transistor is in. an ON state (evidence is shown in the Sasaki reference, USP 5,039,873, that a MOSFET transistor is functionally equivalent to a resistor when the MOSFET transistor is ON, see Figure 4c, and Col. 1, lines 2 1-22 of Sasaki). Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify the above circuitry by substitute an always ON MOSFET transistor (i.e., a MOSFET transistor having a. DC bias at its gate so that the MOSFET transistor is ON) for each of the resistors in the circuitry because they are functionally equivalent and for the purpose that it is easily integrated. With such a modification, the limitation of claim 31 is met as that the RC discriminator including a resistive-transistor and a capacitor (also note that because

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the circuitry is fabricated by using SOI technology as discussed in claim 14, so the body of the SOI transistor is floating with respect to an underlying substrate). Note that, in the above modification, the functional limitation in claim 32 is also met as the operation of control network circuitry modulates the potential voltage of the body and limit the body to a reference voltage. Also, note that the device includes a source S and a drain D (Figure 4b of Au et al), wherein the source is connected to the resistive-transistor (both connected to ground), and the drain is connected to the capacitor as recited in claim 34; and the functional limitation that the resistive transistor and said capacitor initiate coupling of the gate when an over-voltage or over-current condition exits (recited in claim 35) is also met (Col. 5, lines 30-67 of Au et al.) and also because the structure of the RC discriminator connected to the gate of the MOSFET device of the Au et al. is substantially identical as the structure of the RC discriminator of the inventions. Also, Figure 4b of the Au et al. shows a PAD) (PAD) coupled to the capacitor (for claim 36).

With respect to claims 18 and 33, the modification/combination as discussed in claim 31 meets the limitations of these claims that the circuit control network (40, Figure 4b of Au et al.) includes at least a SOI MOSFET because the circuitry is fabricate by using SOI technology (discussed in. claim 14), and because every resistor in the circuitry is formed by using an always ON MOSFET transistor (as discussed in claim 31) so the SOI MOSFET in this claim is the always ON MOSFET transistors for resistors RI and IC in circuit 40 of Figure 4b.

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2. Appellants' Position

a. Independent Claims 14 and 31

i. Lack of Prima Facie Case of Obviousness

The Office Action fails to set forth a prima face case of obviousness. More specifically, the Au reference does not disclose using the claimed "control circuit network" (which provides the electrostatic discharge protection described above) in a floating (silicon-over-insulator) structure. The Office Action argues that, because the Brady reference discloses that silicon-over-insulator structures are well-known, Au could have been used in a silicon-over-insulator structure.

Au would not be operable in a silicon-over-insulator (SOI) structure. When the proposed combination of references destroys the operability of one of the references, this indicates that the proposed combination would not have been made by one ordinarily skilled in the art. Briefly, Au discloses a SCR - a silicon controlled rectifier. SCR's require an N-well for their operation. Without an N-well, SCR's cannot operate. For this simple fact, SCR's cannot be fabricated using SOI technology because there is no N-well in SOI technology. Therefore, using the structure in Au in a SOI structure would destroy the operability of the structure and one ordinarily skilled in the art would not have made the modification suggested in the Office Action.

In response to such a position, the Office Action has stated that Au does not indicate that the SCR could not be used in SOI structures (Office Action, page 8, last line, page 9 first line). In other words, Appellants have demonstrated how the modified device proposed in the rejection is inoperable, and the Office Action has responded by noting that the applied reference does not state that it would be inoperable. This reasoning does not contradict or rebut Appellant's argument because most prior art reference do not discuss in which environments they do not work, but only discuss environments in which

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they do work. Therefore, it would not be expected for the Au reference to explicitly state that it does not work with SOI environments and the lack of any such negative statement does not rebut the argument set forth by Appellants. Thus, the burden is still on the Office to set forth a prima facie case of obviousness (and provide an explanation how SCR's could be used in a SOI environment) especially after Appellants have demonstrated that without an N-well, SCR's cannot operate, and that SCR's cannot be fabricated using SOI technology because there is no N-well in SOI technology.

In addition, the Office Action states that the claims lack a negative limitation regarding the body not being connected to ground potential. The claims should define what the invention is, not what the invention is not, and therefore negative limitations are generally avoided. Further, such a negative limitation is not necessary because this limitation is positively recited by defining that the "body is floating with respect to the underlying substrate." One ordinarily skilled in the art would understand that a floating or SOI structure is not connected to ground potential. Therefore, contrary to the statements in the Office Action, the claimed features are presented as being novel in Appellants' arguments.

The circuit described in Au cannot be utilized in silicon-over-insulator (SOI) by simply stating that (as the Office Action does) because the body of the transistor in Au is controlled by the control circuit 40, when the structure disclosed in Au is constructed using SOI technology, the control circuit 40 will still control the bias of the body. Note that this reasoning does not contradict Appellant's previous explanation that the structure disclosed in Au cannot be constructed using SOI technology. Instead, here the Office Action makes an incorrect presumption that the structure described in Au can be formed using SOI technology. Thus, where the Office Action argues ". . . when the circuitry in Au is fabricated by using SOI technology . . ." the Office Action presents an impossible presumption since the circuitry in Au cannot be fabricated using SOI technology. In other words, the argument that Au is properly combinable with Brady is based upon an incorrect presumption that the circuitry within Au can be fabricated using SOI technology

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(which, as discussed in greater detail below, is incorrect), and therefore, the arguments presented in the Office Action are defective because the teachings from Au cannot be applied to SOI technologies.

Au discloses a SCR - a silicon controlled rectifier (column 4, lines 40-44). More specifically, Au discloses a "low-voltage triggering silicon-controlled rectifier (LVTSCR)" (column 5, lines 5-8). SCR's require an N-well for their operation. Without an N-well, SCR's cannot operate. For this simple fact, SCR's cannot be fabricated using SOI technology because there is no N-well in SOI technology. Therefore, teachings regarding SCR's are simply irrelevant in technologies that utilize SOI.

More specifically, Au contains a PNPN device with a MOSFET that is electrically connected to an N-well and to ground in bulk Silicon (Au Figures 4a-4b). One cannot build a PNPN element in SOI technology because the body is floating with respect to the underlying substrate. A Low Voltage Trigger SCR cannot be built in SOI since LVTSCR circuits require use of a P+ diffusion in an N-well, a MOSFET connected to a well, a substrate region, and a n+ cathode. There is no N-well in SOI technology, hence, an SCR cannot be constructed in SOI. Hence, it would not be obvious to build an SCR in SOI. Au's circuit is electrically connected to the chip substrate. Au is not a triple well technology, and hence it cannot electrically connect to the substrate and have operability. Au also has a resistor, a capacitor, and a pad; however, as shown in Figure 4b of Au, a network exists between the pad 34 and ground potential. To the contrary, with the claimed invention, because of the body is floating with respect to the underlying substrate, the pass transistor is not electrically connected to ground potential.

Therefore, Appellant respectfully submits that the proposed combination of Brady and Au is invalid, since a silicon controlled rectifier cannot be built using SOI technology. Thus, it is Appellant's position that a prima facie case of obviousness has not been set forth because, in this instance, Brady is not properly combinable with Au.

If the device in Au were transferred to the SOI technology field, this would destroy the operability of the device in Au because Au relies on the body being non-

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floating. When the proposed combination of references destroys the operability of one of the references, this indicates that the proposed combination would not have been made by one ordinarily skilled in the art.

Non-SOI structures do not insulate the body from the underlying substrate, while in SOI structures the body is insulated (floating). The technologies with respect to the body potential are fundamentally different, and teachings relating to bodies of non-SOI structures generally cannot be transferred to the floating bodies of SOI structures because of the fundamental difference regarding the body potential. While SOI technologies present substantial advantages over non-SOI technologies (because of the floating body) SOI technologies also present a number of impediments which were not present in non-SOI technologies (also because the body is floating). Generally non-SOI technologies cannot be transferred to SOI technologies. Therefore, simply referring to Brady as disclosing an SOI structure and then concluding that all the non-SOI teachings in Au can readily apply to an SOI structure is not reasonable given that the structure in Au must be modified significantly in order to be functional within the SOI technology environment. Indeed, simply transferring the structure shown in Au to an SOI environment would render the operation of the device in Au non-functional because Au relies upon the body being non-floating in order to have the device properly operate. Thus, because the proposed combination destroys the operability of the Au reference, Appellant submits that a prima facie case of obviousness has not been set forth. This is especially true considering that the claimed invention is directed toward solving problems associated with the potential of the floating body which is a problem unique to SOI structures.

ii. No Teaching of the Claimed Invention

The proposed combination does not teach or suggest the "circuit control network connected to said body, said circuit control network modulating a potential voltage of said body to provide electrostatic discharge (ESD) protection" where the body "is floating

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with respect to an underlying substrate." Because it is improper to modify the Au reference (as shown above) there in no teaching of such features defined by independent claim 1 and 31. Therefore, independent claims 1 and 31 are patentable over the prior art of record and, the Board is respectfully requested to reconsider and withdraw the rejection of claims 14 and 31.

b. Dependent Claims 17, 18, and 32-36

The following discussion demonstrates that the combination of Au and Brady does not teach or suggest the invention defined by the dependent claims, but also that the dependent claims are independently patentable over their associated independent claims and do not stand or fall with their associated independent claims.

Claims 17 and 32 define that the circuit control network limits the body to a reference voltage. As shown above, the teachings of Au cannot transfer to an SOI environment. Therefore, the combined teachings of Au and Brady would not teach or suggest to one ordinarily skilled in the art the features that are defined by dependent claims 17 and 32. Thus, it is Appellants position that dependent claims 17 and 32 are independently patentable on their own over the prior of record.

Claims 18 and 33 define that the circuit control network comprises at least one SOI MOSFET. As shown above, the teachings of Au cannot transfer to an SOI environment. Therefore, the combined teachings of Au and Brady would not teach or suggest to one ordinarily skilled in the art the features that are defined by dependent claims 18 and 33. Thus, it is Appellants position that dependent claims 18 and 33 are independently patentable on their own over the prior of record.

Claim 34 defines a source and a drain, wherein one of the source and the drain is connected to the resistive transistor and the other of the source and the drain is connected to the capacitor. As shown above, the teachings of Au cannot transfer to an SOI environment. Therefore, the combined teachings of Au and Brady would not teach or

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suggest to one ordinarily skilled in the art the feature that is defined by dependent claim 34. Thus, it is Appellant's position that dependent claim 34 is independently patentable on their own over the prior of record.

Claim 35 defines a resistive transistor and the capacitor initiate coupling of the gate when an overvoltage or overcurrent condition exists. As shown above, the teachings of Au cannot transfer to an SOI environment. Therefore, the combined teachings of Au and Brady would not teach or suggest to one ordinarily skilled in the art the features that is defined by dependent claim 35. Thus, it is Appellants position that dependent claim 35 is independently patentable on their own over the prior of record.

Claim 36 defines a pad connected to the capacitor. As shown above, the teachings of Au cannot transfer to an SOI environment. Therefore, the combined teachings of Au and Brady would not teach or suggest to one ordinarily skilled in the art the features that are defined by dependent claim 36. Thus, it is Appellants position that dependent claim 36 is independently patentable on their own over the prior of record.

In view of the foregoing, the Board is respectfully requested to reconsider and withdraw the rejection of claims 17, 18, and 32-36.

C. The Rejection Based on Ker in view of Au and Brady

1. The Position in the Office Action

The Office Action states:

> With respect to claim 24, Figure 2 of the Ker reference discloses a device which includes: an n-channel MOSFET (Mn1) comprising a first body and a first gate; a p-channel MOSFET (Mp1) comprising a second body and a second age; a first RC discriminator comprising a first resistor (Rn) and a first capacitor (Cn1); and a second RC discriminator (Rp, Cp1) comprising a second resistor (Rp) and a second capacitor (Cp1). The Ker reference does not discloses the device a first circuit control network for modulating a

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potential voltage of the first body, and a second circuit control network for modulating a potential voltage of the second body. However, the Au et al. reference discloses in Figure 6 a device that includes first and second circuit control networks (SCR 52 and 50, wherein the detail of the 5CR is shown as circuit 40 in Figure 4b) for controlling the first and second bodies (bodies of Q3 and Q2), respectively for the purpose of improving the level of ESD protection of either a positive or negative polarity ESD event (see line 59 of Col. 5 to line 23 of Col. 6). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to provide the device of Figure 2 of the Ker et al. reference with the first and second circuit control networks connected to the first and second bodies, respectively, for the purpose of improving the level of ESD protection of either a positive or negative polarity ESD event. Thus, this modification meets the limitations of the first and second circuit control networks as recited in claim 24 including the functional limitation "to provide ESD protection".

The combination of the Ker et al. reference and the Au et al. reference meets all the limitations of claim 24 except that the circuitry is fabricated by using silicon-over-insulator SOI technology. However, the Brady et al. reference discloses that silicon-over-insulator (SOI) technology provides advantages over regular silicon technology such as increasing the operating speed and reducing the power consumption of the circuitry (Col. 1, lines 12-15 of Brady et al.). Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify above combination by using specific SOI technology to fabricate the circuitry for the purpose of increasing the operating speed and reducing the power consumption of the circuitry. Thus, this modification meets all the limitation of claim 24. Note that, in this modification, "a fist body that is floating with respect to an underlying substrate" on line 3-4 and "a second body that is floating with respect to said. underlying substrate" on line 6-7 of claim 14 is met when fabricate the device by using SOI technology (i.e., the bodies of Mp1 and Mn1, Figure 2 of Ker et al. in the modification are

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floating with respect to the underlying substrate) because the body of an SOI MOSFET is floating with respect to an underlying substrate.

With respect to claim 26, Figure 2 of the Ker et al. in the above combination shows the n-channel SOI MOSFET Mn1 comprises a source and a drain connected to the first resistor (Rn) and the first capacitor (Cn1); and the p-channel SOI MOSFET transistor includes a source and a drain connected to the second resistor (Rp) and the second capacitor (Cp1).

With respect to claim 27, the functional limitation that the first resistor and capacitor and the second resistor and capacitor initiate coupling of the first gate and the second gate, respectively, when an over-voltage or over-current condition exists is met (see line 65 of Col. 4 to line 5 of Col. 5). Further, because the structure of the first and second RC discriminator circuit connected to the first and second gates is substantially identical to Appellant's invention so it must functions the same.

With respect to claim 28, it is seen in the operation of the combination/modification circuitry that the first circuit control network limits the first body to a reference voltage, and the second circuit control network limits the second body to the reference voltage (both of the circuit control networks SCR in the above combination/modification are the game so they must limit the same reference voltage).

With respect to claim 29, it is seen that the two circuit control networks SCR in the above combination/modification coupled to difference voltages, i.e., the one that is coupled to the body of the p-channel MOSFET is coupled to the power supply voltage, and the one that is coupled to the body of the n-channel MOSFET is coupled to ground.

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With respect to claim 30, the above combination/modification circuitry shows a pad (21, Figure 2 of Ker et al.) connected between the n-channel and p-channel SOI MOSFETs.

With respect to claim 25, the modification/combination of Ker et al., Au et al. and Brady et al. as discussed in claim 24 above meets all the limitations of this claim except that first and second circuit control network comprises at least one SOI MOSFET. However, it is art-recognized that a resistor could be easily implemented in an integrated circuitry by using a transistor that has its gate connected to DC bias so that the transistor is in an ON state (evidence is shown in the Sasaki reference, USP 5,039,873, that a MOSFET transistor is functionally equivalent to a resistor when the MOSFET transistor is ON, see Figure 4c, and Col. 1 lines 21-22 of Sasaki). Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify the above combination or modification circuitry by substitute an always ON MOSFET transistor (i.e., a MOSFET transistor having a DC bias at its gate so that the MOSFET transistor is ON) for each of the resistors in the circuitry because they are functionally equivalent and for the purpose that it is easily integrated. With this modification, the limitations of this claim is met because the first and second circuit control networks (40, Figure 4b of Au et al.) includes at least a SOI MOSFET because the circuitry is fabricate by using SOI technology, and because every resistor in the circuitry is formed by using an always ON MOSFET transistor so the SOI MOSFET in this claim is the always ON MOSFET transistors (for resistors R1 and R2 in circuit 40 of Figure 4b of Au et al.).

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2. Appellants' Position

a. Independent Claim 24

i. Lack of Prima Facie Case of Obviousness

The Office Action fails to set forth a prima face case of obviousness. More specifically, the Au reference does not disclose using the claimed "control circuit network" (which provides the electrostatic discharge protection described above) in a floating (silicon-over-insulator) structure. The Office Action argues that, because the Brady reference discloses that silicon-over-insulator structures are well-known, Au could have been used in a silicon-over-insulator structure.

Appellants have explained above (and the same arguments are incorporated herein by reference) why the circuit described in Au would not be operable in a silicon-over-insulator (SOI) structure. Briefly, Au discloses a SCR - a silicon controlled rectifier. SCR's require an N-well for their operation. Without an N-well, SCR's cannot operate. For this simple fact, SCR's cannot be fabricated using SOI technology because there is no N-well in SOI technology.

In response, the Office Action states that this argument is not persuasive because Au does not indicate that the SCR could not be used in SOI structures (Office Action, page 8, last line, page 9 first line). In other words, Appellants have demonstrated how the device proposed in the rejection is inoperable, and the Office Action has responded by noting that the applied reference does not state that it would be inoperable. This reasoning does not contradict or rebut Appellant's argument because most prior art reference do not discuss in which environments they do not work, but only discuss environments in which they do work. Therefore, it would not be expected for the Au reference to explicitly state that it does not work with SOI environments and the lack of

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any such negative statement does not rebut the argument set forth by Appellants. Thus, the burden is still on the Office to set forth a prima facie case of obviousness (and provide an explanation how SCR's could be used in a SOI environment) especially after Appellants have demonstrated why such a modified structure would not be operable.

Further, Brady is not properly combinable with Au or Ker. The Office Action proposes to combine Brady with Au and Ker to show that the technology within Au and Ker could be extended to SOI technology. However, this combination is not reasonable given that the invention is directed toward controlling the body potential of an SOI transistor and that the teachings of non-SOI technologies are not generally transferable to the floating bodies of SOI structures. Further, as described in detail below, if the devices in Au and Ker were transferred to the SOI technology field, this would destroy the operability of the devices in Au and Ker because Au and Ker rely on the body being non-floating. When the proposed combination of references destroys the operability of one of the references, this indicates that the proposed combination would not have been made by one ordinarily skilled in the art.

As pointed out above, non-SOI structures do not insulate the body from the underlying substrate, while in SOI structures the body is insulated (floating). The technologies with respect to the body potential are fundamentally different, and teachings relating to bodies of non-SOI structures generally cannot be transferred to the floating bodies of SOI structures because of the fundamental difference regarding the body potential. While SOI technologies present substantial advantages over non-SOI technologies (because of the floating body) SOI technologies also present a number of impediments which were not present in non-SOI technologies (also because the body is floating). Generally, non-SOI technologies cannot be transferred to SOI technologies, unless compensation is made for the floating body. Therefore, simply referring to Brady as disclosing an SOI structure and then concluding that all the non-SOI teachings in Au and Ker can readily apply to an SOI structure is not reasonable given that the structures in Au and Ker must be modified significantly in order to be functional within the SOI

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technology environment. Indeed, simply transferring the structures shown in Au and Ker to an SOI environment would render the operation of the devices in Au and Ker non-functional because Au and Ker rely upon the body being non-floating in order to have the devices properly operate. Thus, because the proposed combination destroys the operability of the Au and Ker references, Appellant's submit that a prima facie case of obviousness has not been set forth. This is especially true considering that the claimed invention is directed toward solving problems associated with the potential of the floating body which is a problem unique to SOI structures.

As shown above, Au and Ker are not properly combinable with Brady. There is nothing within Ker or Au that would have suggested to one ordinarily skilled in the art that they should combine Brady with Au and/or Ker. Therefore, this rejection is similarly defective as the previous rejection in that a prima facie case of obviousness has not been set forth. In view of the foregoing, the Board is respectfully requested to reconsider and withdraw the rejection of claim 24.

ii. No Teaching of the Claimed Invention

The proposed combination does not teach or suggest the "circuit control network connected to said body" where the "circuit control network modulating a potential voltage of said [first/second] body to provide electrostatic discharge (ESD) protection" where the body "is floating with respect to an underlying substrate." Because it is improper to modify the Au reference (as shown above) there in no teaching of such features defined by independent claim 24. Therefore, independent claim 24 is patentable over the prior art of record and, the Board is respectfully requested to reconsider and withdraw the rejection of claim 24.

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b. Dependent Claims 25-30

The following discussion demonstrates that the combination of Ker, Au and Brady does not teach or suggest the invention defined by the dependent claims 25-30, but also that the dependent claims are independently patentable over their associated independent claims and do not stand or fall with their associated independent claims.

Claim 25 defines a first circuit control network and the second circuit control network comprise at least one SOI MOSFET. The Examiner combines Ker with Au. The Office Action admits that Ker does not disclose the device a first circuit control network, nor a second control network that discloses a second device. One cannot combine Ker with Au and Brady, since Au is a SCR for switching an SCR, and Ker is bulk CMOS, and Brady is SOI. One cannot map the solution of Au into Ker and Brady, since it would not be operable nor possible to design and implement. Hence it would not be obvious to combine Ker, Brady and Au. Further, Sasaki uses an RC network which is connected to a pad, a resistor, a capacitor and this is electrically connected to the gate of a MOSFET between the pad and ground potential. Thus, Sasaki teaches gate modulation and not body modulation.

As shown above, Au and Ker are not properly combinable with Brady. The Office Action makes reference to Sasaki for the limited purpose of disclosing a resistive transistor and there is nothing within Sasaki that would have suggested to one ordinarily skilled in the art that they should combine Brady and Au and Ker. Therefore, this rejection is similarly defective as the previous rejection in that a prima facie case of obviousness has not been set forth. In view of the foregoing, the Board is respectfully requested to reconsider and withdraw the rejection of claim 25.

Claim 26 defines the n-channel SOI MOSFET further comprises a first source and a first drain, wherein one of the first source and the first drain is connected to the first resistor and the other of the first source and the first drain is connected to the first

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capacitor; and wherein the p-channel SOI MOSFET further comprises a second source and a second drain, wherein one of the second source and the second drain is connected to the second resistor and the other of the second source and the second drain is connected to the second capacitor. As shown above, Au and Ker are not properly combinable with Brady. Therefore, the combined teachings of Ker, Au and Brady would not teach or suggest to one ordinarily skilled in the art the features that is defined by dependent claim 26. Thus, it is Appellant's position that dependent claim 26 is independently patentable on their own over the prior of record.

Claim 27 defines the first resistor and the first capacitor initiate coupling of the first gate when an overvoltage or overcurrent condition exists; and wherein the second resistor and the second capacitor initiate coupling of the second gate when the overvoltage or overcurrent condition exists. As shown above, Au and Ker are not properly combinable with Brady. Therefore, the combined teachings of Au and Brady would not teach or suggest to one ordinarily skilled in the art the features that are defined by dependent claim 27. Thus, it is Appellant's position that dependent claim 27 is independently patentable on their own over the prior of record.

Claim 28 defines the first circuit control network limits the first body to a reference voltage, and the second circuit control network limits the second body to the reference voltage. As shown above, Au and Ker are not properly combinable with Brady. Therefore, the combined teachings of Au and Brady would not teach or suggest to one ordinarily skilled in the art the features that are defined by dependent claim 28. Thus, it is Appellant's position that dependent claim 28 is independently patentable on their own over the prior of record.

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Claim 29 defines the first circuit control network and the second control network are coupled to different reference voltages. As shown above, Au and Ker are not properly combinable with Brady. Therefore, the combined teachings of Au and Brady would not teach or suggest to one ordinarily skilled in the art the features that are defined by dependent claim 29. Thus, it is Appellant's position that dependent claim 29 is independently patentable on their own over the prior of record.

Claim 30 defines a pad connected between the n-channel SOI MOSFET and the p-channel SOI MOSFET. As shown above, Au and Ker are not properly combinable with Brady. Therefore, the combined teachings of Au and Brady would not teach or suggest to one ordinarily skilled in the art the features that are defined by dependent claim 30. Thus, it is Appellant's position that dependent claim 30 is independently patentable on their own over the prior of record.

As shown above independent claim 24 is patentable over the prior art of record. Further, dependent claims 26-30 are similarly patentable, not only because they depend from a patentable claim, but also because of the additional features of the invention they define. In view of the foregoing, the Board is respectfully requested to reconsider and withdraw the rejection of claims 26-30.

VIII. CONCLUSION

In view the forgoing, the Board is respectfully requested to reconsider and withdraw the rejections of claims 14, 17, 18, and 24-36.

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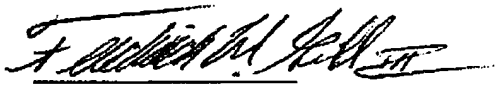
10/631,098
Appeal Brief

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,



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VIII. CLAIMS APPENDIX

1-13 (Canceled).

14. (Previously Presented) A silicon over-insulator (SOI) metal oxide silicon field effect transistor (MOSFET) device comprising:

a body that is floating with respect to an underlying substrate;

a gate opposite said body;

an RC discriminator comprising a resistor and a capacitor, wherein said RC discriminator is connected to said gate at a point of said RC discriminator between said resistor and said capacitor; and

a circuit control network connected to said body, said circuit control network modulating a potential voltage of said body to provide electrostatic discharge (ESD) protection.

15. (Withdrawn) The device in claim 14, wherein said circuit control network is connected to said gate.

16. (Canceled).

17. (Previously Presented) The device in claim 14, wherein said circuit control network limits said body to a reference voltage.

18. (Previously Presented) The device in claim 14, wherein said circuit control network comprises at least one SOI MOSFET.

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19. (Withdrawn) The device in claim 14, wherein said circuit control network comprises at least one ESD SOI diode.

20. (Withdrawn) The device in claim 14, wherein said circuit control network comprises at least one body/gate-coupled SOI diode.

21. (Canceled).

22. (Withdrawn) The device in claim 14, further comprising:

an input pad connected to said gate;

a drain adjacent said gate; and

a source opposite said drain,

wherein said circuit control network is connected to said input pad and said drain and said source is connected to Vss.

23. (Canceled).

24. (Previously Presented) A silicon over insulator (SOI) metal oxide silicon field effect transistor (MOSFET) device comprising:

an n-channel SOI MOSFET comprising a first body that is floating with respect to an underlying substrate and a first gate opposite said first body;

a p-channel SOI MOSFET connected to said n-channel SOI MOSFET, wherein said p-channel SOI MOSFET comprises a second body that is floating with respect to said underlying substrate and a second gate opposite said second body;

a first RC discriminator comprising a first resistor and a first capacitor, wherein said first RC discriminator is connected to said first gate at a point of said first RC discriminator between said resistor and said capacitor;

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a second RC discriminator comprising a second resistor and a second capacitor, wherein said second RC discriminator is connected to said second gate at a point of said second RC discriminator between said resistor and said capacitor;

a first circuit control network connected to said first body, said first circuit control network modulating a potential voltage of said first body to provide electrostatic discharge (ESD) protection; and

a second circuit control network connected to said second body, said second circuit control network modulating a potential voltage of said second body to provide electrostatic discharge (ESD) protection.

25. (Previously Presented) The device in claim 24, wherein said first circuit control network and said second circuit control network comprise at least one SOI MOSFET.

26. (Previously Presented) The device in claim 24, wherein said n-channel SOI MOSFET further comprises a first source and a first drain, wherein one of said first source and said first drain is connected to said first resistor and the other of said first source and said first drain is connected to said first capacitor; and

wherein said p-channel SOI MOSFET further comprises a second source and a second drain, wherein one of said second source and said second drain is connected to said second resistor and the other of said second source and said second drain is connected to said second capacitor.

27. (Previously Presented) The device in claim 24, wherein said first resistor and said first capacitor initiate coupling of said first gate when an overvoltage or overcurrent condition exists; and

wherein said second resistor and said second capacitor initiate coupling of said second gate when said overvoltage or overcurrent condition exists.

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28. (Previously Presented) The device in claim 24, wherein said first circuit control network limits said first body to a reference voltage, and said second circuit control network limits said second body to said reference voltage.

29. (Previously Presented) The device in claim 24, wherein said first circuit control network and said second control network are coupled to different reference voltages.

30. (Previously Presented) The device in claim 24, further comprising a pad connected between said n-channel SOI MOSFET and said p-channel SOI MOSFET.

31. (Previously Presented) A silicon over insulator (SOI) metal oxide silicon field effect transistor (MOSFET) device comprising:

a silicon-over-insulator body that is floating with respect to an underlying substrate;

a gate opposite said body;

an RC discriminator comprising a resistive transistor and a capacitor, wherein said RC discriminator is connected to said gate at a point of said RC discriminator between said resistive transistor and said capacitor; and

a circuit control network connected to said body, said circuit control network modulating a potential voltage of said body to provide electrostatic discharge (ESD) protection.

32. (Previously Presented) The device in claim 31, wherein said circuit control network limits said body to a reference voltage.

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33. (Previously Presented) The device in claim 31, wherein said circuit control network comprises an SOI MOSFET.

34. (Previously Presented) The device in claim 31, further comprising a source and a drain, wherein one of said source and said drain is connected to said resistive transistor and the other of said source and said drain is connected to said capacitor.

35. (Previously Presented) The device in claim 31, wherein said resistive transistor and said capacitor initiate coupling of said gate when an overvoltage or overcurrent condition exists.

36. (Previously Presented) The device in claim 31, further comprising a pad connected to said capacitor.

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IX. EVIDENCE APPENDIX

There is no other evidence known to Appellants, Appellant's' legal representative or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

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X. RELATED PROCEEDINGS APPENDIX

There is no other related proceedings known to Appellants, Appellant's' legal representative or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

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APR 14 2006

TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. BUR919990193US2

In Re Application Of: **Steven H. Voldman**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/631,098	July 31, 2003	Long T. Nguyen	29154	2816	7752

Invention: **SOI VOLTAGE-TOLERANT BODY-COUPLED PASS TRANSISTOR**

COMMISSIONER FOR PATENTS:

Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed on:

The fee for filing this Appeal Brief is: **$500.00**

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